REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3, 5, and 14-16 are presently active. Claims 1, 2, and 5 have been amended; and Claims 14-16 have been added by the present amendment. The changes and additions to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claim 2 was rejected under 35 U.S.C. § 112, second paragraph, regarding the phrase "first plating layer is a conductive substrate." In addition, Claims 1-3 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,642,160 to Burgess (hereinafter "the '160 patent") in view of U.S. Patent No. 5,747,358 to Gorrell et al. (hereinafter "the '358 patent").

Amended Claim 1 is directed to a printed wiring board, comprising: (1) an insulating layer having a first surface and a second surface; (2) a plurality of circuit patterns formed by etching metal foils laminated on at least the first surface and the second surface of the insulating layer; (3) a via formed on said insulating layer, the via having one end opened on the first surface of the insulating layer, and the other end closed by a circuit pattern of the plurality of circuit patterns formed on a part of the insulating layer other than the first surface; (4) a first plating layer having a first portion that covers an inner surface of the via and the circuit pattern that closes the other end of the via and which is exposed within the via, and a second portion that covers a circuit pattern of the plurality of circuit patterns that is on the first surface and which continues to the one end of the via; and (5) a second plating layer laminated on the first plating layer and electrically connecting a circuit pattern formed on the first surface with the circuit pattern that closes the other end of the via. Claim 1 has been amended for the purposes of clarification only and no new matter has been added.

Regarding the rejection of Claim 1 under 35 U.S.C. § 103(a), the Office Action asserts that the '160 patent discloses everything in the claims with the exception of the second plating layer, and relies on the '358 patent to remedy that deficiency.

The '160 patent is directed to a circuit board including an insulating layer having a first surface and a second surface, a plurality of wiring layers laminated on the first and second surfaces, and a via formed on the insulating layer. Layer 38 of the '160 patent establishes an electrical connection between the wiring layer exposed within the via and the wiring layers on the first and second surfaces.

Initially, Applicants note that layer 38 remains on the wiring layers even after the manufacturing of the circuit board is completed, as shown in Figure 9 of the '160 patent. Accordingly, the thickness of the circuit pattern is increased by the thickness of layer 38. Thus, the '160 patent fails to recognize the problem addressed by the present application, namely the need for making the circuit pattern exposed on the outside of the circuit board *thinner*. Moreover, as noted in the Office Action, the '160 patent fails to disclose a second plating layer laminated on the first plating layer and electrically connecting a circuit pattern on the first surface with a circuit pattern that closes the other end of the via, as recited in amended Claim 1.

The '358 patent is directed to a method of forming raised metallic contacts on electrical circuits. In particular, the metal layer disclosed in Figure 16 of the '358 patent establishes an electrical connection between (1) the pads and (2) the circuit board and the conductive layer that forms the bump 50. However, the metal layer does not establish an electrical connection between the circuit pattern on the first surface and the circuit pattern that closes the other end of the via, as recited in amended Claim 1. Specifically, note that the copper conductive layers 12 and 16 shown in Figure 1 are removed in the step in which the

bump 50 is formed.[3] Moreover, Applicants note that the plurality of layers of gold, copper, and nickel laminated on top of each other are exposed to the outside of the circuit board in the vicinity of the bump 50 and the via 40. Accordingly, as with the '160 patent, the '358 patent fails to recognize the problem addressed by the present invention, namely the need to make the circuit patterns thinner.

Thus, no matter how the teachings of the '160 and '358 patents are combined, the combination does not teach or suggest a second plating layer laminated on a first plating layer and electrically connecting a circuit pattern formed on the first surface with the circuit pattern that closes the other end of the via, as recited in amended Claim 1. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established, and that the rejection of Claim 1 (and dependent Claims 2, 3, and 5) should be withdrawn.

The present amendment also sets forth new Claims 14-16 for examination on the merits. New Claims 14-16, which depend from Claim 1, are supported by the originally filed specification and do not add new matter.[4] Moreover, based on their dependence from Claim 1, Applicants respectfully submit that Claims 14-16 patentably define over the '160 and '358 patents.

Thus, it is respectfully submitted that independent Claim 1 (and dependent Claims 2, 3, 5, and 14-16) patentably define over the '160 and '358 patents.

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[3]See Figures 9 and 10 of the '358 patent.

[4]See, for example, Figure 1 and page 23 of the specification.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599
Surinder Sachar
Registration No. 34,423

22850

(703) 413-3000
GJM/SNS/KMB/sy

I:\atty\kmb\210854us\210854US-am.wpd

Marked-Up Copy
Serial No: 09/899,156
Amendment filed
11-14-02

IN THE SPECIFICATION

Please amend the paragraph at page 23, lines 4-13, as follows:

The inner surface of the via 7 is covered with a first plating layer 8. The first plating layer 8 functions as a [conductive substrate] groundwork for conductivity. The first plating layer 8 continuously covers the rear surface of the wiring layer 4 exposed within the via 7. The first plating layer 8 has a flange portion 9 extending to the first surface 2a of the insulating layer 2 from the one end 7a of the via 7. The flange portion 9 covers a portion continuing to the one end 7a of the via 7 out of the wiring layer 3.

IN THE CLAIMS

Please amend Claims 1, 2, and 5 as follows:

1. (Twice Amended) A printed wiring board, comprising:

an insulating layer having a first surface, and a second surface located on [the] an opposite side of said first surface;

a plurality of [wiring layers formed so as to correspond to a predetermined circuit pattern, said wiring layers being laminated at least on said first surface and said second surface of said insulating layer] circuit patterns formed by etching metal foils laminated on at least said first surface and said second surface of said insulating layer;

a via formed on said insulating layer, said via having one end opened on said first surface of said insulating layer and an [the] other end closed by a circuit pattern of said plurality of [wiring layer] circuit patterns formed [laminated] on a part of said insulating layer other than said first surface;

a first plating layer[, said first plating layer continuously covering said inner surface of said via, said wiring layer exposed within said via and that portion of the wiring layer which is formed on said first surface and which faces on end of said via] having (1) a first portion that covers an inner surface of said via and a circuit pattern of said plurality of circuit patterns that closes said other end of said via and which is exposed within said via, and (2) a second portion that covers a circuit pattern of said plurality of circuit patterns that is on said first surface and which continues to said one end of said via; and

a second plating layer[, said second plating layer being] laminated on said first plating layer[,] and electrically connecting a circuit pattern of said [wiring layer] plurality of circuit patterns formed on said first surface [and] with said circuit pattern of the plurality of circuit patterns that closes said other end of said via [said wiring layer laminated on the part of said insulating layer other than said first surface by cooperating with said first plating layer].

2. (Amended) The printed wiring board according to claim 1, wherein said first plating layer [is a conductive substrate] is a groundwork on which said second plating layer is formed, and gives conductivity to the inner surface of said via.

5. (Twice Amended) The printed wiring board according to claim 1, wherein said insulating layer and said [wiring layer] plurality of circuit patterns form a laminate, and

one of said [wiring layers] plurality of circuit patterns is formed inside insulating layer, is exposed within said via, and is covered by said first plating layer.

14-16. (New)